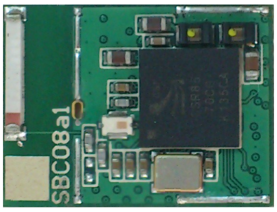
CSR8670 Bluetooth Modules

SBC2015



Preliminary Specification

Version 1.0

24-JAN.-2013

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Documentation History

Revision	Description	Date	Remark
V0.1	SBC1713 preliminary released	JUNE 2012	
V0.2	Add pin G3. PCB dimension changed. Model name change to SBC2015	JULY 2012	
V0.3	Operating Termperature changed.	JAN. 2013	
V1.0	NFC function added	APR. 2013	

內容目錄

1. Description

SBC2015 audio transmitter/Receiver is power by CSR BC8670 technology. That provides a complete 2.4GHz Bluetooth technology for stereo music transmission. The SBC2015 module is compliant with Bluetooth specification v3.0 EDR ,4.0 LE and support A2DP, AVRCP, HSP, HFP, and MAP, SPP, PBAP under request. It is the 10dBm module with build in antenna. Reduce the effort on the l s it into the system. Smart Design also customize the software to meet the require

2. Features

CSR BlueCore8670 Chip.

Bluetooth v3.0 EDR, Bluetooth 4.0 BLE Compliant.

Bluetooth 10dBm RF output power. 10~50 meters transmission distance.

Updated 80 MHz DSP performance.

two digital microphone input.

Three touch sensor input.

Three LED driver.

USB and UART digital interface.

Supported A2DP1.2, HSP1.2, HFP1.6(HD voice ready) , AVRCP 1.4 ,PBAP1.0 and SPP1.0 Profile MAP1.0(SMS notification) under reqeust.

Fully configurable with simple AT style commands over UART and Bluetooth connections.

Build in high performance chip antenna.

Integrated high quality stereo ADC and DAC.

Dimension: 20.8 X 15.4 X 3mm.

LGA(Land Grid Array) pads reliable PCB mounting.

NFC tag supported.

BQE、FCC certified.

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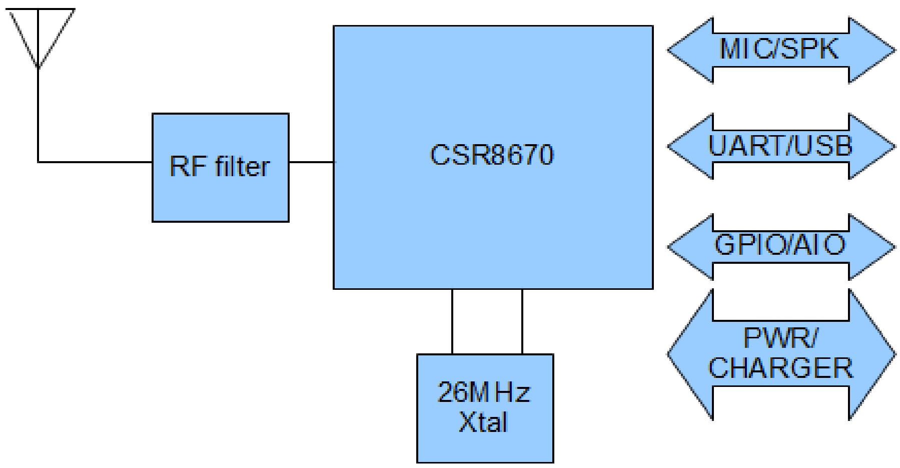
3. Block Diagram



SBC2015 Module Block Diagram

4. Radio Characteristics

	Frequency (GHz)	MIN	TYP	MAX	BT Spec	Unit
Sensitivity at 0.1%BER	2.402	≤-93	-85	-	<= -70	dBm
	2.441	≤-93	-85	-		dBm
	2.480	≤-93	-85	-		dBm
RF Transmit Power	2.402	0	3	10	<= 4	dBm
	2.441	0	3	10		dBm
	2.480	0	3	10		dBm
Initial Carrier Frequency Tolerance	2.402	-	5	75	75	kHz
	2.441	-	5	75		kHz
	2.480	-	5	75		kHz
20dB bandwidth for modulated carrier		-	900	1000	<=1000	kHz
Drift (Five slots packet)		-	15	-	40	kHz
Drift Rate		-	13	-	20	kHz
Δf1 avg “Maximum Modulation”	2.402	140	165	175	140 < Δf1 avg	kHz
	2.441	140	165	175		kHz
	2.480	140	165	175		kHz
Δf2 max “Minimum Modulation”	2.402	115	190	-	115	kHz
	2.441	115	190	-		kHz
	2.480	115	190	-		kHz

5. Electrical Characteristics

Power Consumption

DUT Role	Connection		Packet Type	Average Current	Unit
N/A	Deep sleep	With UART host connection	-	55	µA
N/A	Page scan	Page = 1280ms interval Window = 11.25ms	-	219	µA
N/A	Inquiry and page scan	Inquiry = 1280ms interval Page = 1280ms interval Window = 11.25ms	-	378	µA
Master	ACL	Sniff = 500ms, 1 attempt, 0 timeout	DH1	119	µA
Master	ACL	Sniff = 1280ms, 8 attempts, 1 timeout	DH1	109	µA
Master	SCO	Sniff = 100ms, 1 attempt, PCM	HV3	7.6	mA
Master	SCO	Sniff = 100ms, 1 attempt, mono audio codec	HV3	9.8	mA
Master	eSCO	Setting S3, sniff = 100ms, PCM	2EV3	5.8	mA
Master	eSCO	Setting S3, sniff = 100ms, PCM	3EV3	5.4	mA
Master	eSCO	Setting S3, sniff = 100ms, mono audio codec	2EV3	7.9	mA
Master	eSCO	Setting S3, sniff = 100ms, mono audio codec	3EV3	7.5	mA
Slave	ACL	Sniff = 500ms, 1 attempt, 0 timeout	DH1	127	µA
Slave	ACL	Sniff = 1280ms, 8 attempts, 1 timeout	DH1	129	µA
Slave	SCO	Sniff = 100ms, 1 attempt, PCM	HV3	7.8	mA
Slave	SCO	Sniff = 100ms, 1 attempt, mono audio codec	HV3	10	mA
Slave	eSCO	Setting S3, sniff = 100ms, PCM	2EV3	6.2	mA
Slave	eSCO	Setting S3, sniff = 100ms, PCM	3EV3	5.8	mA
Slave	eSCO	Setting S3, sniff = 100ms, mono audio codec	2EV3	8.2	mA
Slave	eSCO	Setting S3, sniff = 100ms, mono audio codec	3EV3	7.9	mA

Conditions

Current consumption values are taken with:

- VBAT pin = 3.7V
- Firmware ID = 7919
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH off

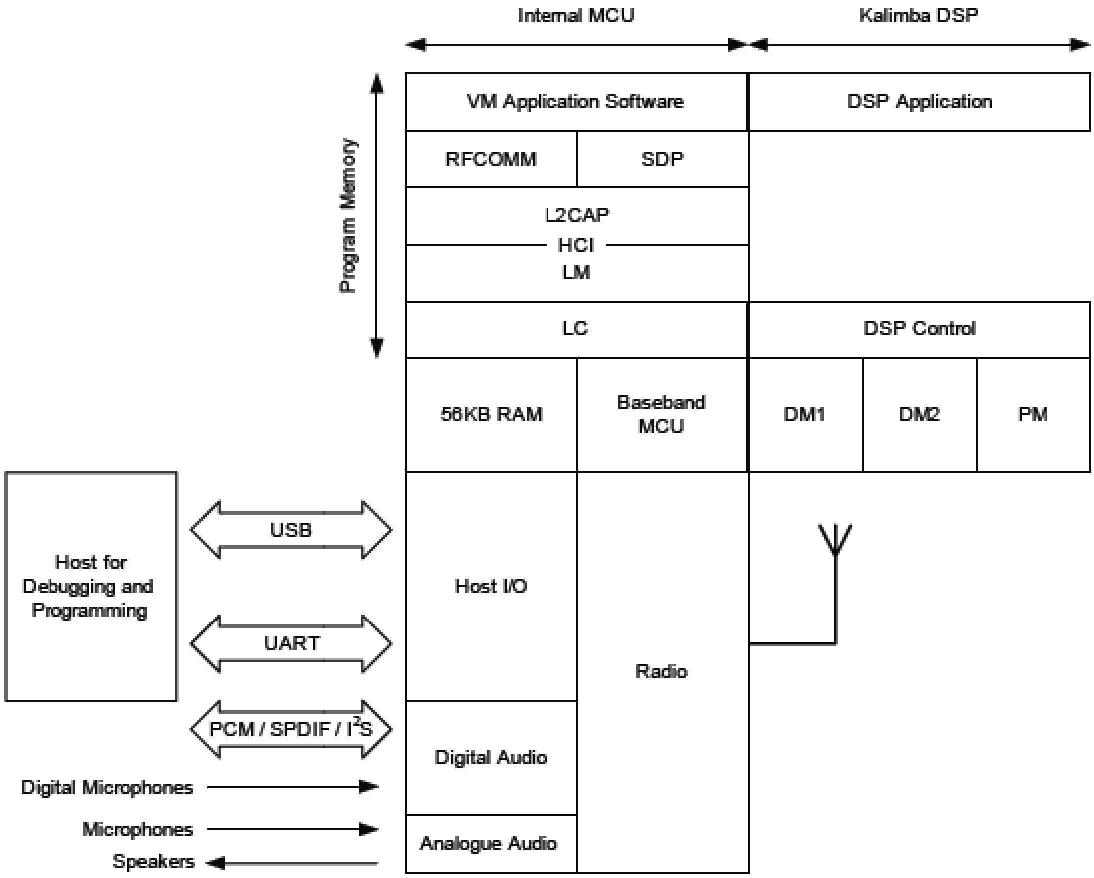
Voltage Input

	MIN	Typ.	MAX	Unit
Supply Voltage	**3.1**	**3.3**	**3.5**	**V**

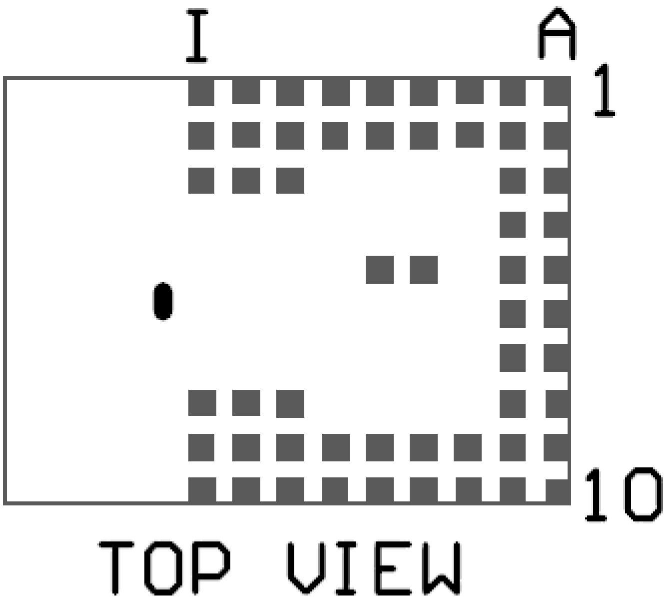
Operating Conditions

Voltage Range	3.3V±0.2V
Operating Temperature Range	-30°C ~ 80°C
Storage Temperature Range	-30°C ~ 85°C
Relative Humidity (Operating)	<=90%
Relative Humidity (Storage)	<=90%

6. Software Diagram



7. Pin Definition



PIN	Name	Type	Note
A1	MIC_LN	I	Microphone input negative, left
A2	MIC_LP	I	Microphone input positive, left
A3	MIC_BIAS_A	PWR	Microphone bias A
A4	MIC_BIAS_B	PWR	Microphone bias B
A5	MIC_RP	I	Microphone input positive, right
A6	MIC_RN	I	Microphone input negative, right
A7	SPKR_RP	O	Speaker output positive, right
A8	SPKR_RN	O	Speaker output negative, right
A9	SPKR_LN	O	Speaker output negative, left
A10	SPKR_LP	O	Speaker output positive, left
B1	VDD_USB	PWR	Positive supply for USB ports
B2	PIO7	I/O	General purpose I/O
B3	PIO4	I/O	General purpose I/O
B4	PIO5	I/O	General purpose I/O
B5	PIO6	I/O	General purpose I/O
B6	PIO3	I/O	General purpose I/O
B7	PIO1	I/O	General purpose I/O
B8	PIO2	I/O	General purpose I/O
B9	PIO0	I/O	General purpose I/O
B10	SPI_CS	I	Chip select for SPI, active low
C1	SMP_VBAT	PWR	1.8V and 1.35V switch-mode power supply regulator inputs. Must be at the same potential as VBAT.
C2	USB_N	I/O	USB data minus
C9	PIO31/LED2	I/O	LED driver. Alternative function PO[31].
C10	SPI_MISO	O	SPI data output

D1	SMPS_3V3	PWR	1.8V and 1.35V switch-mode power supply regulator inputs. Must be at the same potential as VBAT.
D2	USB_P	I/O	USB data plus with selectable internal 1.5kΩ pull-up resistor
D5	GND	PWR	Ground
D9	PIO30/LED1	I/O	LED driver. Alternative function PO[30].
D10	SPI_MOSI	I	SPI data input
E1	VBAT	PWR	Battery positive terminal
E2	VOUT_3V3	PWR	3.3V bypass linear regulator output
E5	GND	PWR	Ground
E9	PIO29/LED0	I/O	LED driver. Alternative function PO[29].
E10	SPI_CLK	CLK	SPI clock
F1	VBAT_SENSE	PWR	Battery charger sense input
F2	VREGENABLE	I	Regulator enable input
F9	PCM_OUT	O	Synchronous data output. Alternative function PIO[18].
F10	UART_RX	I	UART data input.
G1	VCHG	PWR	Battery charger input
G2	RST#	I	Reset if low. Input debounced so must be low for >5ms to cause a reset.
G3	VOUT_1V8	PWR	1.8V bypass linear regulator output
G8	CAP_SENSOR_2	I	Capacitive touch sensor input
G9	PCM_SYNC	I/O	Synchronous data sync. Alternative function PIO[19].
G10	UART_TX	O	UART data output.
H1	CHG_EXT	PWR	External battery charger control
H2	VDD_PADS	PWR	1.7V to 3.6V positive supply input for input/output ports: ■ RST# ■ UART ■ PCM ■ SPI ■ PIO[all]
H3	GND	PWR	Ground
H8	CAP_SENSOR_0	I	Capacitive touch sensor input
H9	PCM_CLK	I/O	Synchronous data clock. Alternative function PIO[20].
H10	UART_CTS	I/O	UART clear to send, active low.
I1	AIO0	I/O	Analogue programmable input / output line
I2	AIO1	I/O	Analogue programmable input / output line
I3	GND	PWR	Ground
I8	CAP_SENSOR_1	I	Capacitive touch sensor input
I9	PCM_IN	I/O	Synchronous data input. Alternative function PIO[17].
I10	PIO16/UART_RTS	I/O	UART request to send, active low. Alternative function PIO[16].

VCC3.3

Supply voltage connection for the digital I/Os of the module. Supply voltage at this pinwith 3.3 V.

GND

Connect GND pins to the ground plane of the PCB.

VDD_BAT

Input for an internal 1.8 V switched mode regulator combined with output of the internal battery charger. When not powered from a battery, VCC3.3 and VDD_BAT can be combined to a single 3.3 V supply voltage.

RST#

The RESET pin is an active low reset.

PIO0 – PIO7

Programmable digital I/O lines. All PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. Configuration for each PIO line depends on the application. Please check Default configuration in Standard Setup Information.

AIO0,1

AIO can be used to monitor analogue voltages such as a temperature sensor for the battery charger. AIO can also be configured to be used as digital I/Os. The default setting is None function.

UART_RTS

A CMOS output with a weak internal pull-up. This pin can be used to implement RS232 hardware flow control where RTS (request to send) is an active low indicator. The UART interface requires an external RS232 transceiver chip.

UART_CTS

A CMOS input with a weak internal pull-down. This pin can be used to implement RS232 hardware flow control where CTS (clear to send) is an active low indicator. The UART interface requires an external RS232 transceiver chip.

UART_RX

A CMOS input with a weak internal pull-down. RXD is used to implement UART data transfer from another device to MB-C05. The UART interface requires an external RS232 transceiver chip.

UART_TX

A CMOS output with a weak internal pull-up. TXD is used to implement UART data transfer from MB-C05 to another device. The UART interface requires external RS232 transceiver chip.

PCM_OUT

A CMOS output with a weak internal pull-down. Used in the PCM (pulse code modulation) interface to transmit digitized audio. The PCM interface is shared with the I^2S interface.

PCM_IN

A CMOS input with a weak internal pull-down. Used in the PCM interface to receive digitized audio. The PCM interface is shared with the I^2S interface.

PCM_CLK

A bi-directional synchronous data clock signal pin with a weak internal pull-down. PCMC is used in the PCM interface to transmit or receive the CLK signal. MB-C05 configured as a slave, the PCMC is an input and receives the clock signal from another device. The PCM interface is shared with the I^2S interface.

PCM_SYNC

A bi-directional synchronous data strobe with a weak internal pull-down. MB-C05 configured as a slave, the PCMS is an input and receives the SYNC signal from another device. The PCM interface is shared with the I^2S interface.

USB_P

A bi-directional USB data line with a selectable internal 1.5 kΩ pull-up implemented as a current source An external series resistor is required to match the connection to the characteristic impedance of the USB cable.

USB_N

bi -directional USB data line. An external series resistor is required to match the connection to the characteristic impedance of the USB cable.

SPI_CSB

A CMOS input with a weak internal pull-down.

SPI_CLK

A CMOS input for the SPI clock signal with a weak internal pull-down.

SPI_MISO

An SPI data output with a weak internal pull-down.

SPI_MOSI

An SPI data input with a weak internal pull-down.

SPKR_RP and SPKR_RN

Right channel audio output. The audio output lines should be routed differentially to either the speakers or to the output amplifier, depending on whether or not a single-ended signal is required. Use low impedance ground plane dedicated for the audio signals.

SPKR_LP and SPKR_LN

Left channel audio output. The same guidelines apply to this section as discussed previously.

MIC_BIAS_A,B

Bias voltage output for a microphone. Use the same layout guidelines as discussed previously with other audio signals.

MIC_RP and MIC_RN

Right channel audio inputs. This dual audio input can be configured to be either single ended or fully differential and programmed for either microphone or line input. Route differential pairs close to each other and use a solid dedicated audio ground plane for the audio signals.

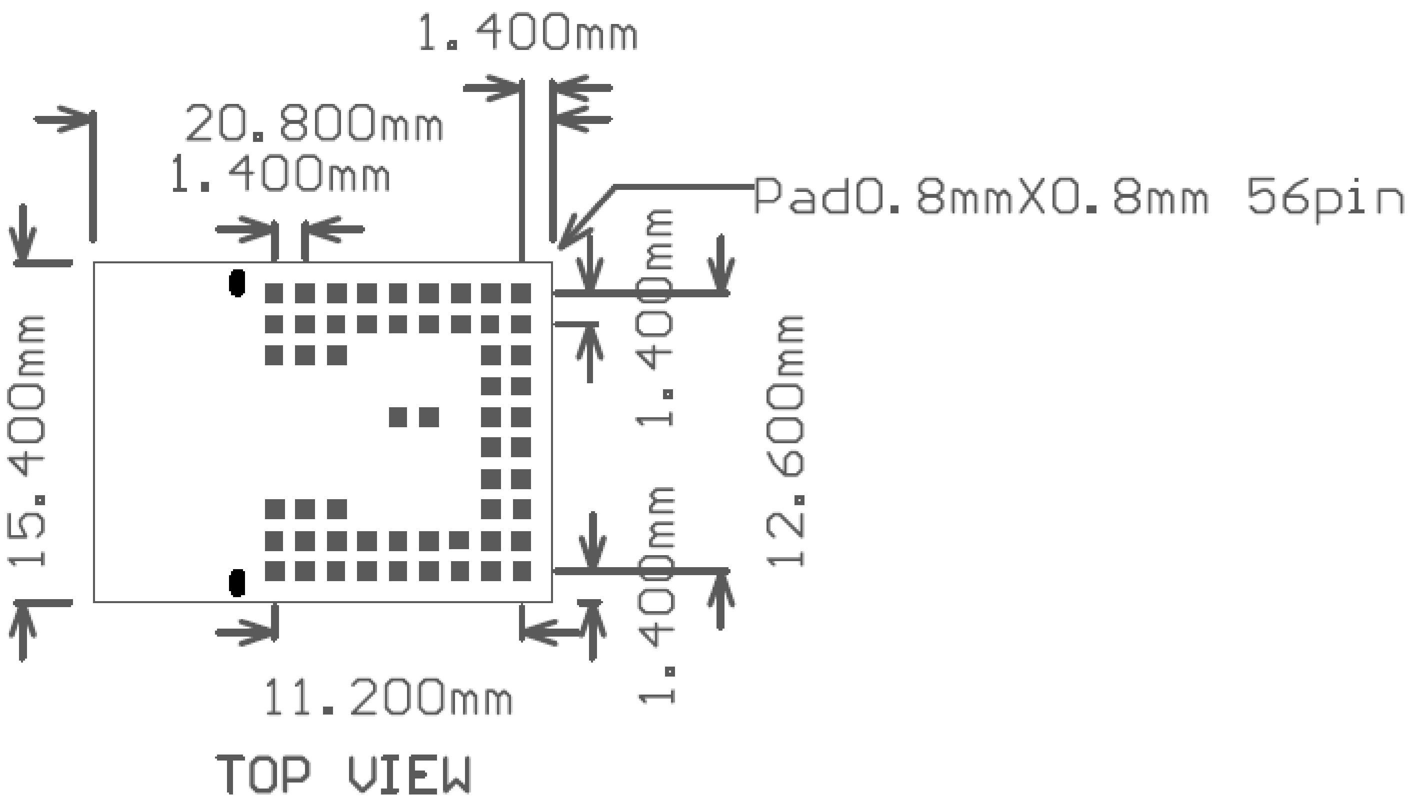
MIC_LP and MIC_LN

Left channel audio input. The same guidelines apply to this section as discussed previously.

CAP_SENSOR

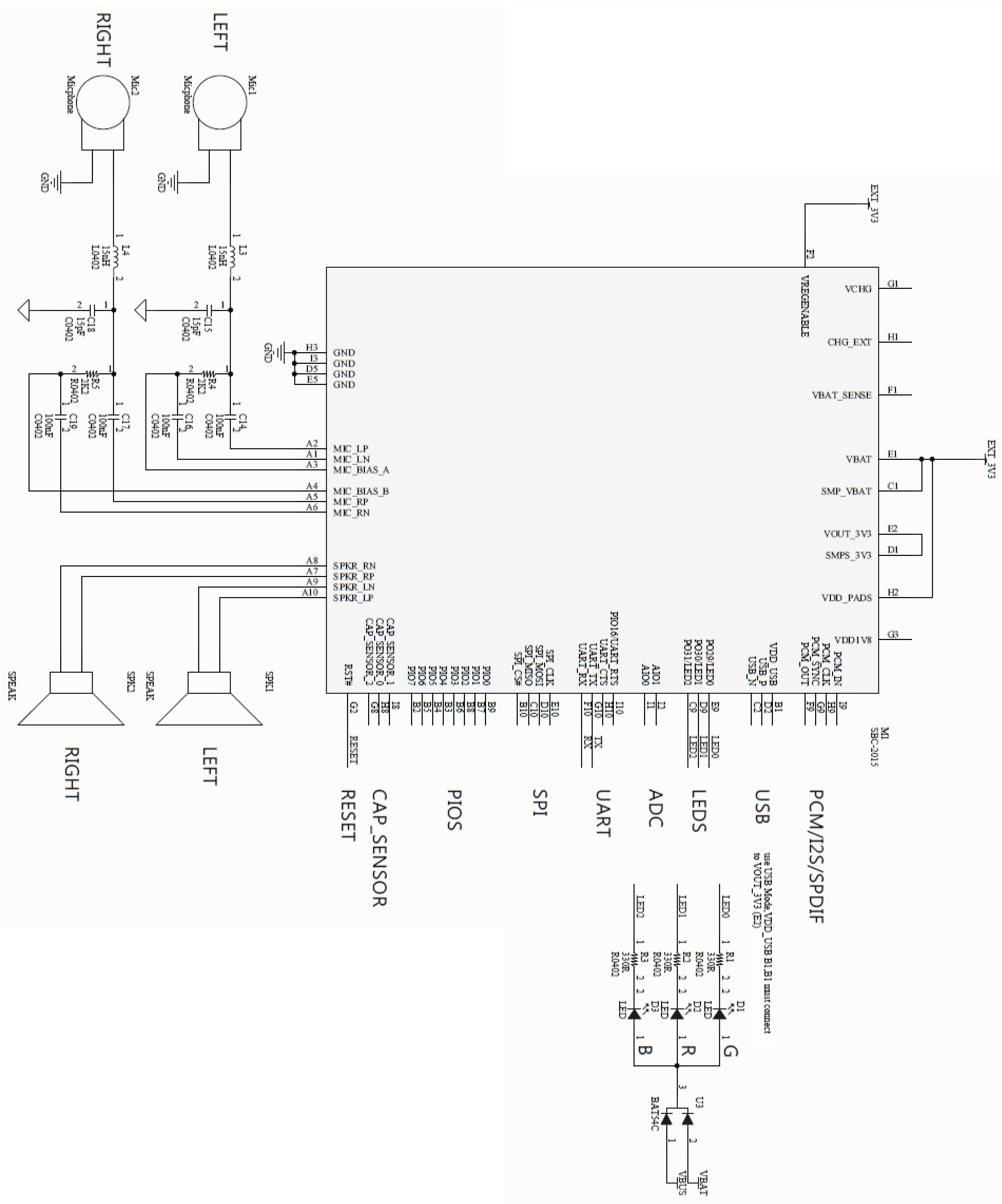
The capacitive touch sensor interface.

8. Mechanical Specification

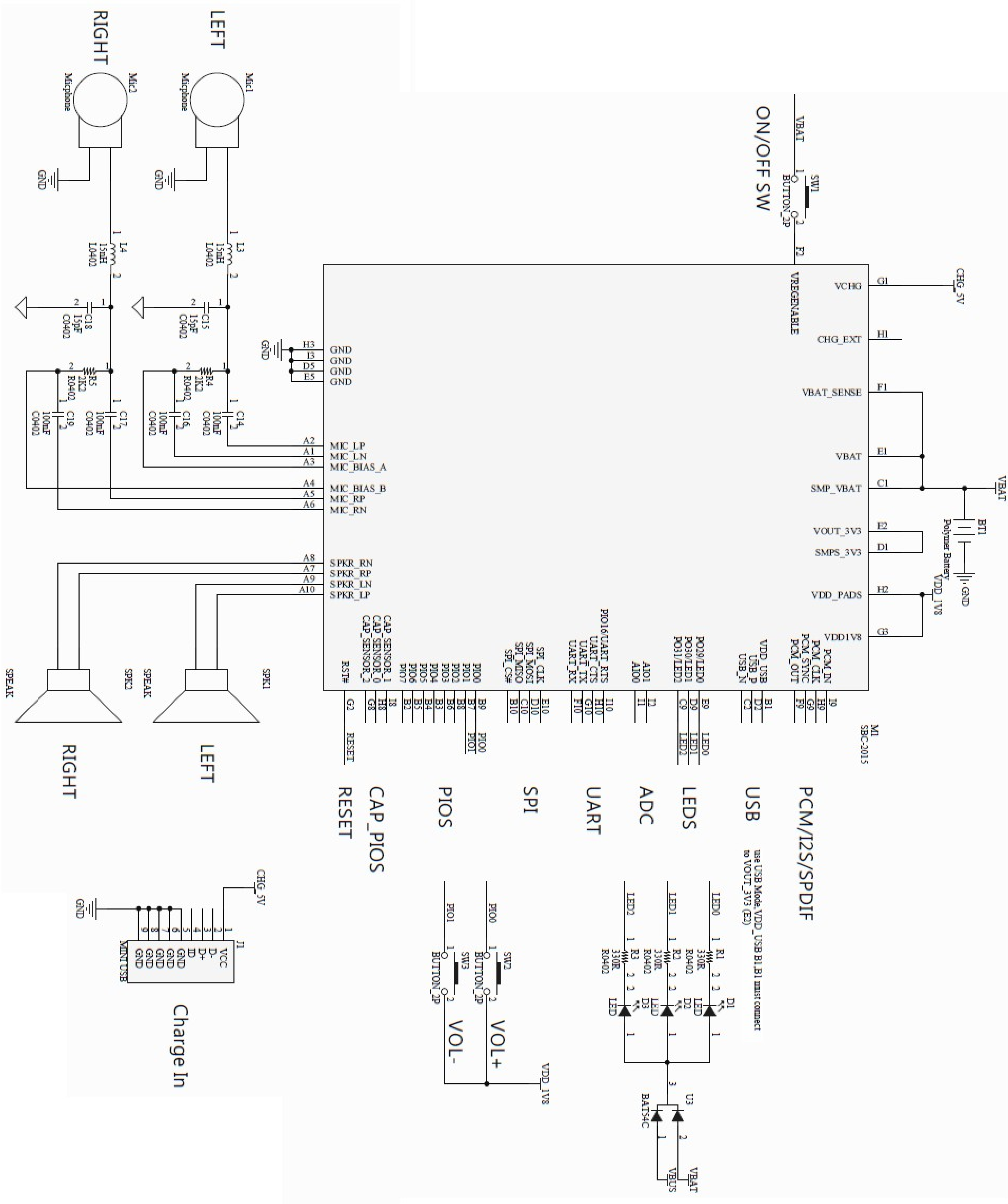


9. Reference Schematics

W/O Battery

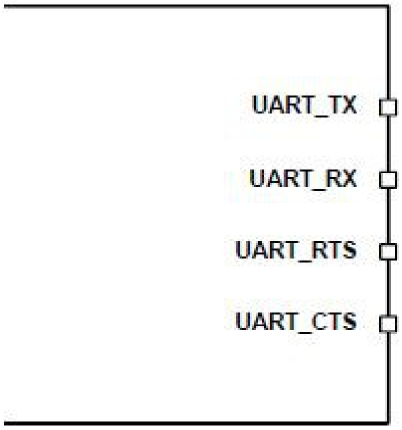


With Battery



10. UART Interface

This is a standard UART interface for communicating with other serial devices. SBC2015 UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.



Universal Asynchronous Receiver

Four signals implement the UART function, . When SBC2015 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. UART configuration parameters, such as baud rate and packet format, are set using SBC2015 firmware.

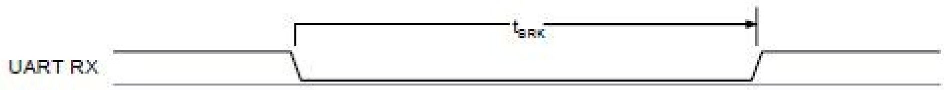
Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Possible UART Settings

The UART interface can reset SBC2015 on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure. If tBRK is longer than the value, defined by the PS Key PSKEY_HOSTIO_UART_RESET_TIMEOUT, (0x1a4), a reset occurs. This feature allows a host to initialise the system to a known state. Also, SBC2015 can emit a break character that may be used to wake the host.



Break Signal

Refer to PSKEY_UART_BITRATE for more information about the baud rates and their values. Generated baud rate is independent of selected incoming clock frequency.

11. USB Interface

This is a full speed (12Mbits/s) USB interface for communicating with other compatible digital devices. SBC2015 acts as a USB peripheral, responding to requests from a master host controller such as a PC. The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported.

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O

buffers of the SBC2015, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

Note:

The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth v2.1 + EDR

specification or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers. As USB is a master/slave oriented system (in common with other USB peripherals), SBC2015 only supports USB Slave operation.

USB Pull-up Resistor

SBC2015 has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on SBC2015 BGA acts as a USB peripheral, responding to requests from a master host controller. SBC2015 supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification) and USB Battery Charging Specification , available from http://www.usb.org. For more information on how to integrate the USB interface on SBC2015 see the Bluetooth and USB Design Considerations Application Note .

As well as describing USB basics and architecture, the application note describes:
■ Power distribution for high and low bus-powered configurations
■ Power distribution for self-powered configuration, which includes USB VBUS monitoring
■ USB enumeration
■ Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
■ USB suspend modes and Bluetooth low-power modes:
■ Global suspend
■ Selective suspend, includes remote wake
■ Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
■ Suspend mode current draw
■ PIO status in suspend mode
■ Resume, detach and wake PIOs
■ Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
■ USB termination when interface is not in use
■ Internal modules, certification and non-specification compliant operation

12. Serial Peripheral Interface

The primary function of the SPI is for debug. SBC2015 uses a 16-bit data and 16-bit address SPI, where transactions may occur when the internal processor is running or is stopped. This section details the interface considerations for connection to SBC2015. Data may be written or read one word at a time, or the auto-increment feature is available for block access.

Instruction Cycle

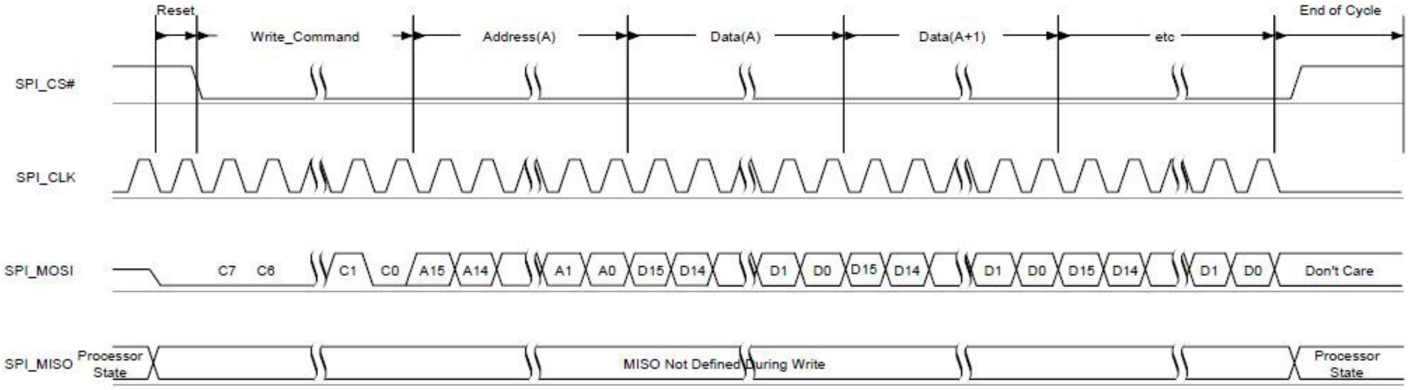
The SBC2015 is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the SBC2015 on the rising edge of the clock line SPI_CLK. When reading, SBC2015 replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The

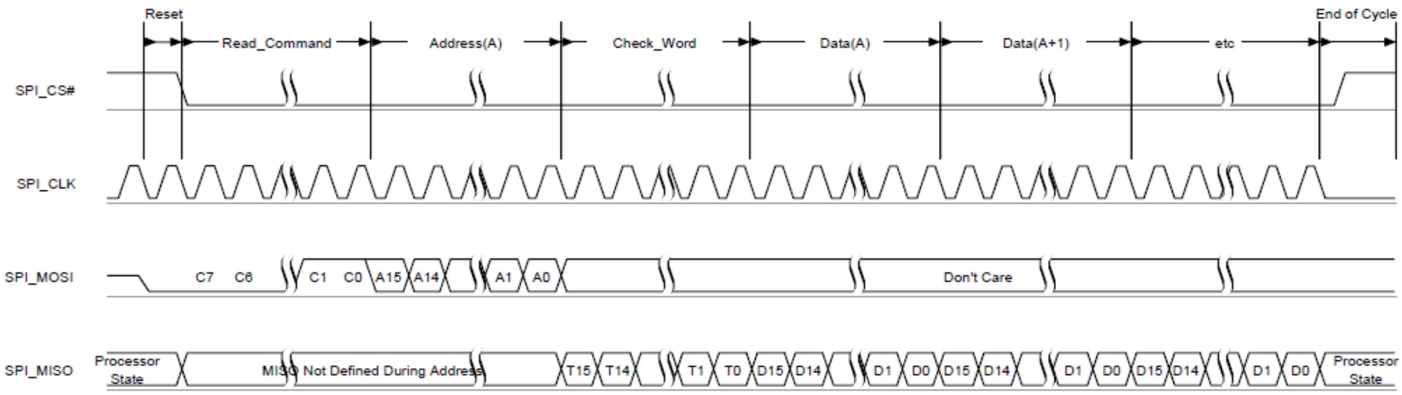
master provides the clock on SPI_CLK.
Taking SPI_CS# high terminates the transaction. Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when transferring large amounts of data. To overcome this SBC2015 offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.
Avoid connecting SBC2015 in a multi-slave arrangement by simple parallel connection of slave MISO lines. When SBC2015 is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, SBC2015 outputs 0 if the processor is running or 1 if it is stopped.



SPI Write Operation

Reading from the Device

Reading from SBC2015 is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). SBC2015 then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0]. The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, wereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the save device not responding.
If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.



SPI Read Operation

13. Audio Interface

The audio interface circuit consists of:

■ Stereo/dual-mono audio codec

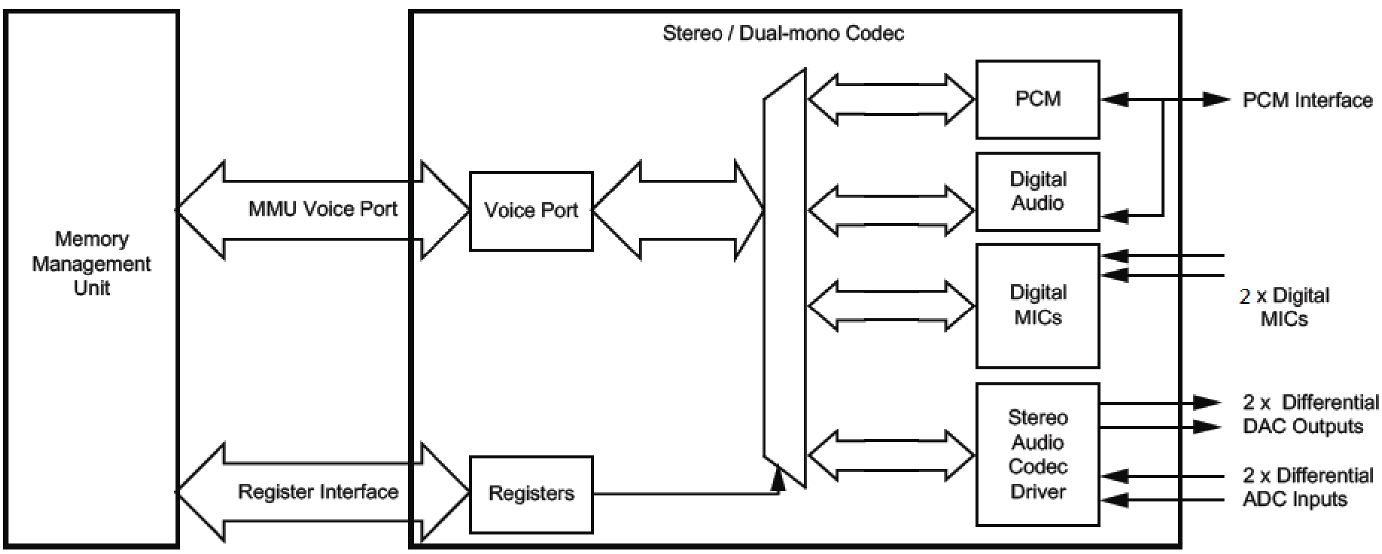
■ Dual analogue audio inputs

■ Dual analogue audio outputs

■ 2 digital MEMS microphone inputs

■ A configurable PCM, I²S or SPDIF interface

Figure shows the functional blocks of the interface. The codec supports stereo/dual-mono playback and recording of audio signals at multiple sample rates with a 16-bit resolution. The ADC and the DAC of the codec each contain 2 independent high-quality channels. Any ADC or DAC channel runs at its own independent sample rate.



Audio Interface

The interface for the digital audio bus shares the same pins as the PCM codec interface which means each of the audio buses are mutually exclusive in their usage.

PCM Interface	SPDIF Interface	I^2S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC	-	WS
PCM_CLK	-	SCK

Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Audio Input and Output

The audio input circuitry consists of:

■ 2 independent 16-bit high-quality ADC channels:

■ Programmable as either microphone or line input

■ Programmable as either stereo or dual-mono inputs

■ Multiplexed with 2 of the digital microphone inputs,

■ Each channel is independently configurable to be either single-ended or fully differential

■ Each channel has an analogue and digital programmable gain stage for optimisation of different microphones

SBC2015 is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

14. Stereo Audio Codec Interface

The main features of the interface are:

■ Stereo and mono analogue input for voice band and audio band

■ Stereo and mono analogue output for voice band and audio band

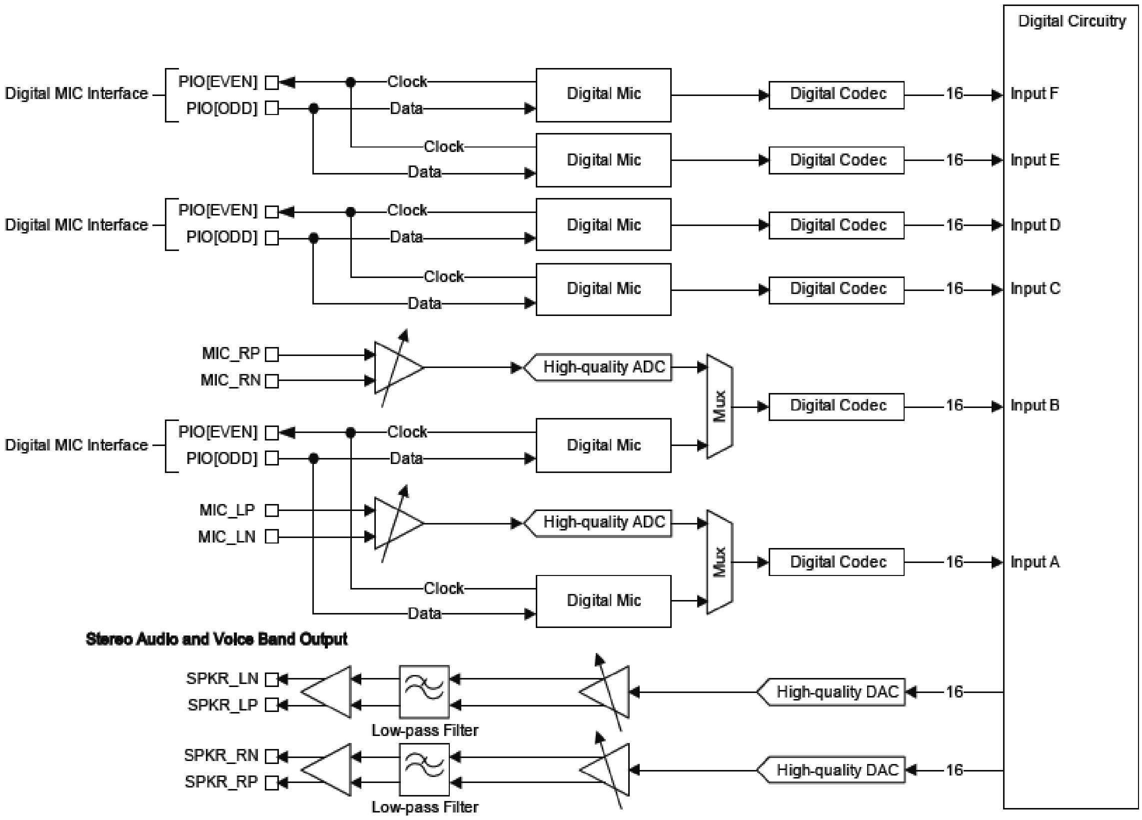
■ Support for stereo digital audio bus standards such as I2S

■ Support for IEC-60958 standard stereo digital audio bus standards, e.g. S/PDIF and AES3/EBU

■ Support for PCM interfaces including PCM master codecs that require an external system clock

Important Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio input and output. With respect to software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel for both input and output.



Stereo Codec Audio Input and Output Stages

The Stereo audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude.

Codec Set-up

The configuration and control of the ADC is through software functions described in appropriate development kit
documentation. This section is an overview of the parameters set up using the software functions.
The Kalimba DSP communicates its codec requirements to the MCU, and therefore also to the VM, by exchanging
messages. Messages between the Kalimba DSP and the embedded MCU are based on interrupts:

■ 1 interrupt between the MCU and Kalimba DSP
■ 1 interrupt between the Kalimba DSP and the MCU

Message content is transmitted using shared memory. There are VM and DSP library functions to send and receive
messages; see appropriate development kit documentation for further details.

ADC

The ADC consists of:

■ Two second-order Sigma Delta converters allowing two separate channels that are identical in functionality.

■ Two gain stages for each channel, one of which is an analogue gain stage and the other is a digital gain stage.

ADC Sample Rate Selection

Each ADC supports the following sample rates:

■ 8kHz
■ 11.025kHz
■ 16kHz
■ 22.050kHz
■ 24kHz
■ 32kHz
■ 44.1kHz
■ 48kHz

DAC

The DAC consists of:

■ Two second-order Sigma Delta converters allowing two separate channels that are identical in functionality.
■ Two gain stages for each channel, one of which is an analogue gain stage and the other is a digital gain stage.

DAC Sample Rate Selection

Each DAC supports the following samples rates:

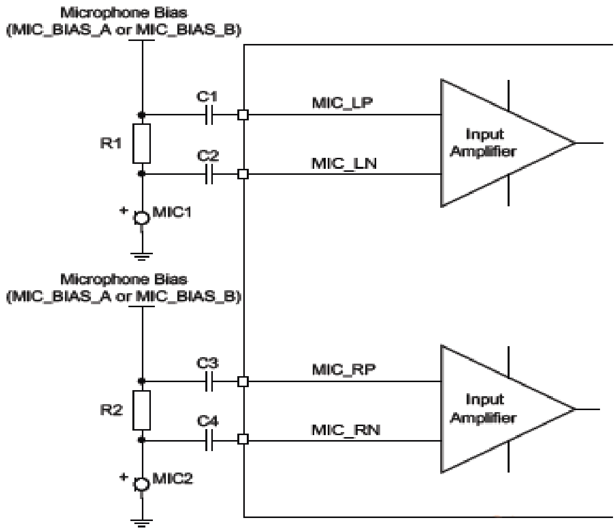
■ 8kHz
■ 11.025kHz
■ 16kHz
■ 22.050kHz
■ 32kHz
■ 40kHz
■ 44.1kHz
■ 48kHz
■ 96kHz

15. Microphone Input

SBC2015 contains 2 independent low-noise microphone bias generators. The microphone bias generators are recommended for biasing electret condensor microphones. Figure 9.6 shows a biasing circuit for microphones with a sensitivity between about -40 to -60dB (0dB = 1V/Pa).
Where:

■ The microphone bias generators derives their power from VBAT (via SMP_VBAT) or VOUT_3V3 (via SMPS_3V3) and requires no capacitor on its output.

■ The microphone bias generators maintains regulation within the limits 70μA to 2.8mA, supporting a 2mA source typically required by 2 electret condensor microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.
■ Biasing resistors R1 and R2 equal 2.2kΩ.
■ The input impedance at MIC_LN, MIC_LP, MIC_RN and MIC_RP is typically 6kΩ.
■ C1, C2, C3 and C4 are 100/150nF if bass roll-off is required to limit wind noise on the microphone.
■ R1 and R2 set the microphone load impedance and are normally around 2.2kΩ.



The microphone bias characteristics include:
■ Power supply:
■ SBC2015 microphone supply is VBAT (via SMP_VBAT) or VOUT_3V3 (via SMPS_3V3)
■ Minimum input voltage = Output voltage + drop-out voltage
■ Maximum input voltage is 4.25V
■ Drop-out voltage:
■ 300mV maximum
■ Output voltage:
■ 1.8V or 2.6V
■ Tolerance 90% to 110%
■ Output current:
■ 70μA to 2.8mA
■ No load capacitor required

Digital Microphone Inputs

SBC2015 interfaces to 2 digital MEMS microphones.
the digital microphone interface on the SBC2015 has:
■ Clock lines shared between 2 microphone outputs, linked to any even-numbered PIO pin as

determined by the firmware.

Note:

Multiple digital microphones can share the same clock if they are configured for the same frequency, e.g. 1 clock for 6 digital microphones.

■ Data lines shared beween 2 microphone inputs, linked to any odd-numbered PIO as determined by the firmware.

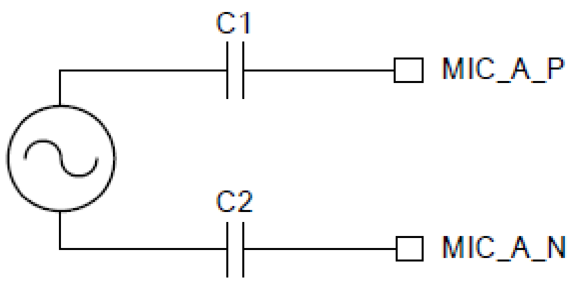
Note:

For the digital microphone interface to work in this configuration ensure the microphone uses a tristate between edges.

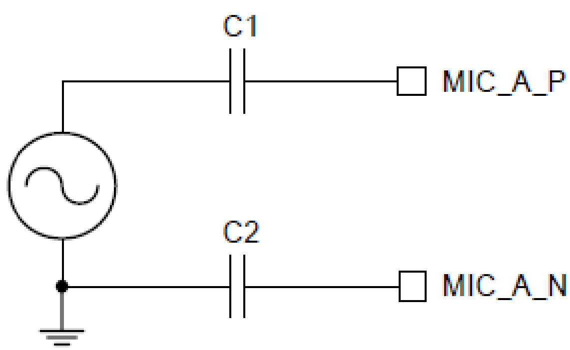
■ The left and right selection for the digital microphones are appropriately pulled up or down for selection on the PCB.

Line Input

If the input analogue gain is set to less than 24dB, SBC2015 automatically selects line input mode. In line input mode the first stage of the amplifier is automatically disabled, providing additional power saving. In line input mode the input impedance varies from 6kΩ - 30kΩ, depending on the volume setting.



Differential Input (Single Channel Shown)

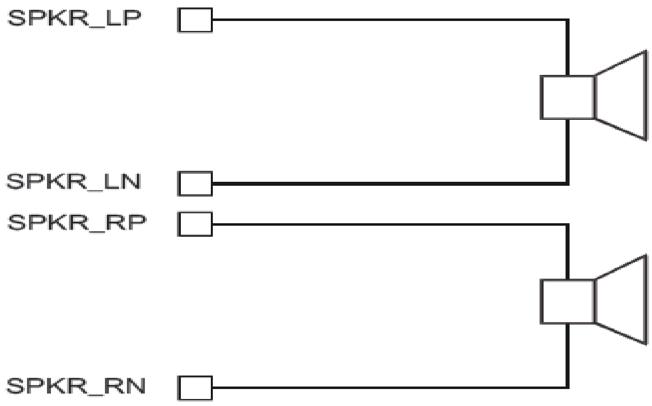


Single-Ended Input (Single Channel Shown)

Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. Figure 9.9 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.



Speaker Output (Single Channel Shown)

Mono Operation

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

16. PCM Interface

The audio PCM interface on the SBC2015 supports:

■ On-chip routing to Kalimba DSP

■ Continuous transmission and reception of PCM encoded audio data over Bluetooth.

■ Processor overhead reduction through hardware support for continual transmission and reception of
PCM data

■ A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not
pass through the HCI protocol layer.

■ Hardware on the SBC2015 for sending data to and from a SCO connection.

■ Up to 3 SCO connections on the PCM interface at any one time.

■ PCM interface master, generating PCM_SYNC and PCM_CLK.

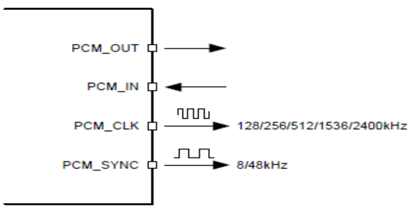
■ PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.

■ Various clock formats including:
■ Long Frame Sync
■ Short Frame Sync
■ GCI timing environments
■ 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
■ Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

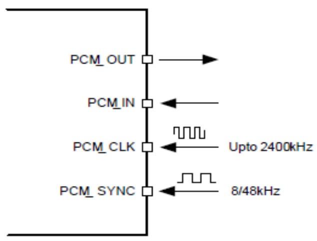
The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

PCM Interface Master/Slave

When configured as the master of the PCM interface, SBC2015 generates PCM_CLK and PCM_SYNC.



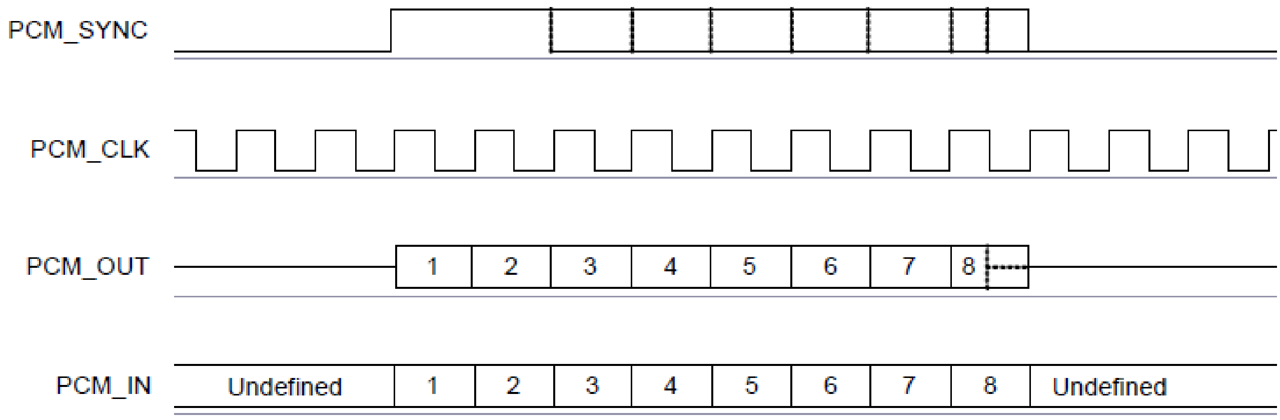
Master



Slave

Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When SBC2015 is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When SBC2015 is configured as PCM Slave, PCM_SYNC is from 1 cycle PCM_CLK to half the PCM_SYNC rate.

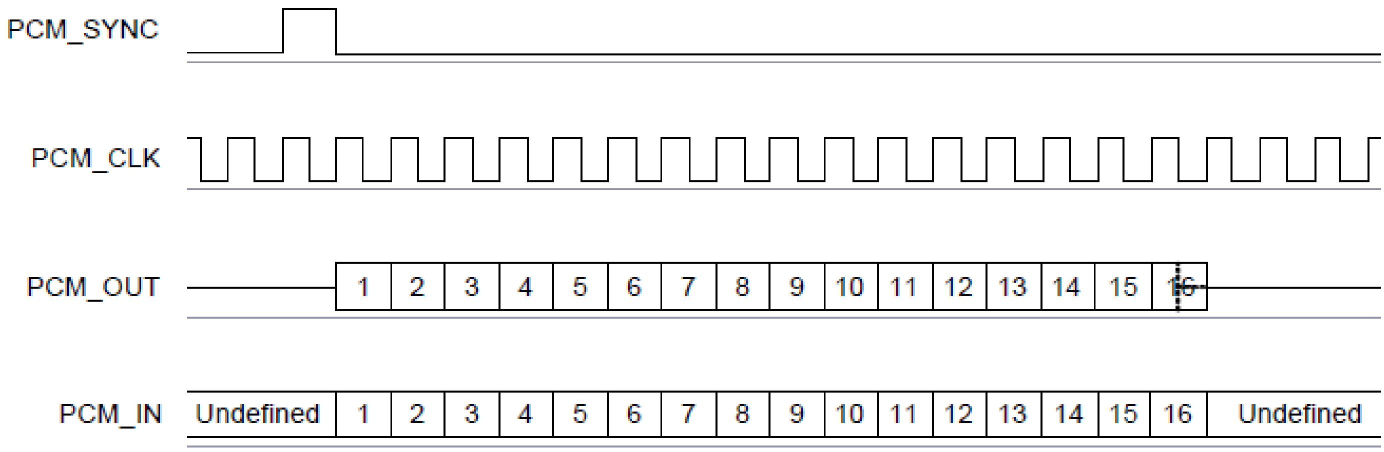


Long Frame Sync (Shown with 8-bit Companded Sample)

SBC2015 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

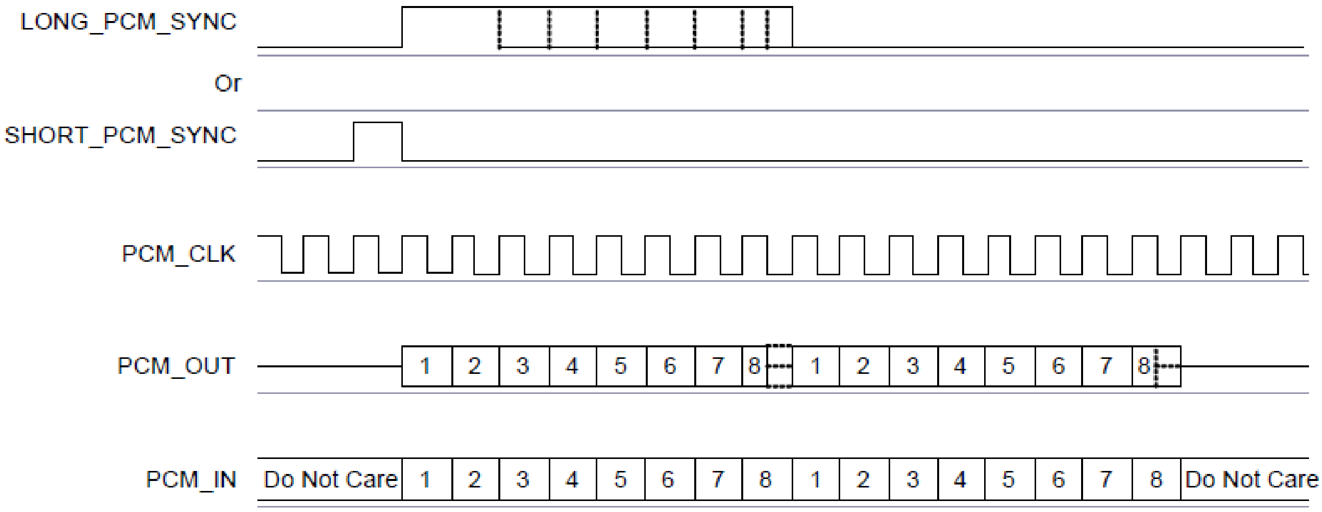


Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, SBC2015 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCOconnections can be carried over any of the first four slots.



Multi-slot Operation with Two Slots and 8-bit Companded Samples

PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Section 9.3.10.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Selection of frequency is programmable. See Section 9.3.10.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} [(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [(a)]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		20	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		0	-	-	ns

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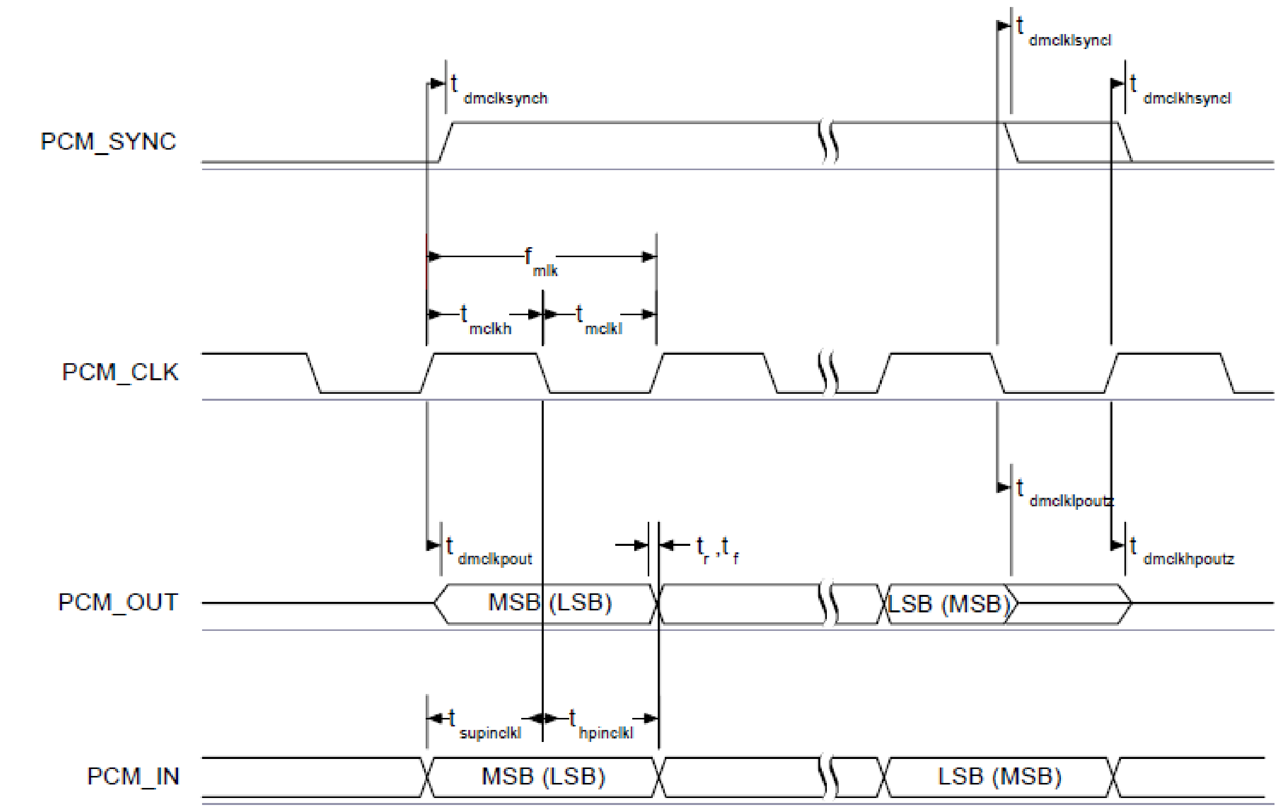
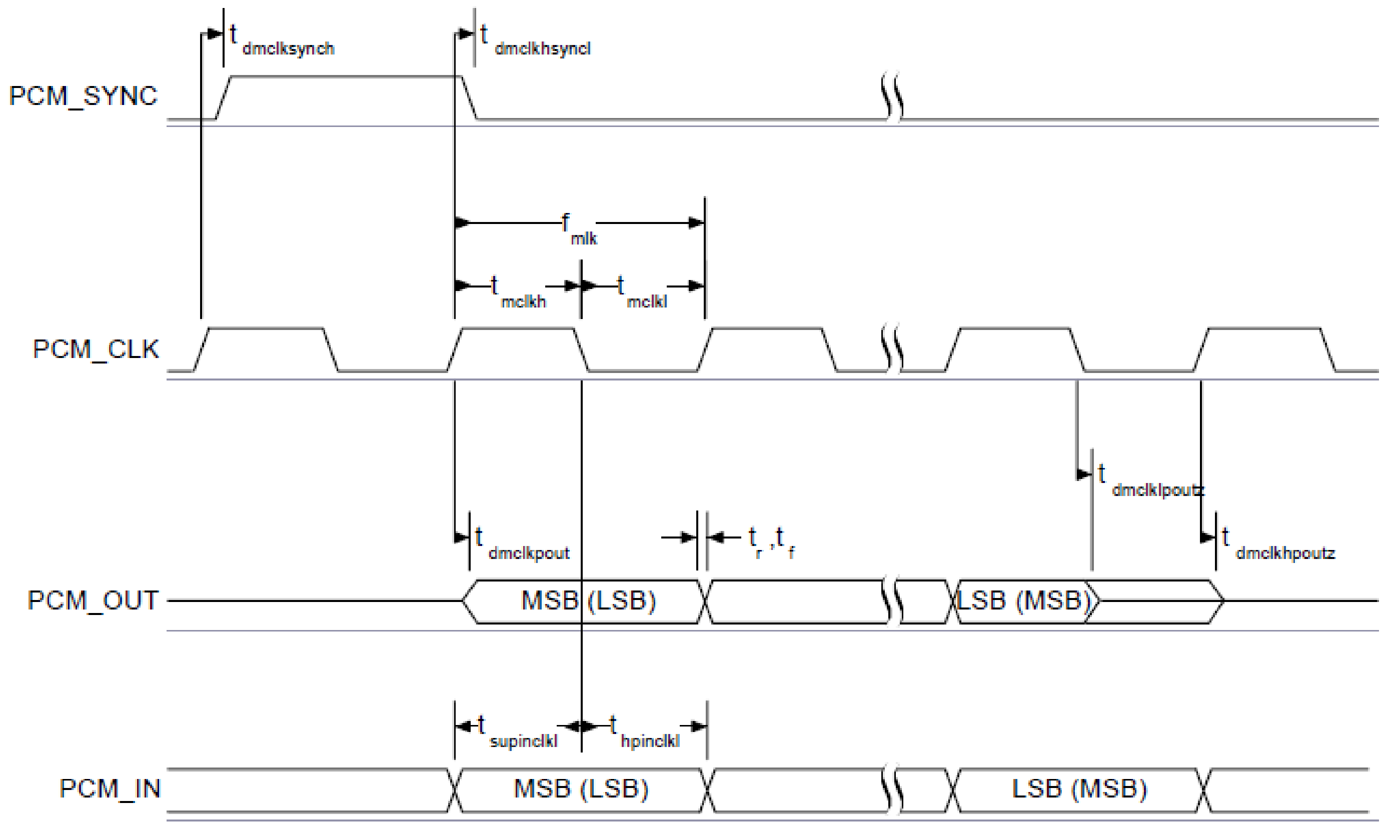


PCM Master Timing Long Frame Sync



PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	(a)	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	(b)	kHz
t_{sclkl}	PCM_CLK low time	80	-	-	ns
t_{sclkh}	PCM_CLK high time	80	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	20	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	20	-	-	ns

PCM Slave Timing

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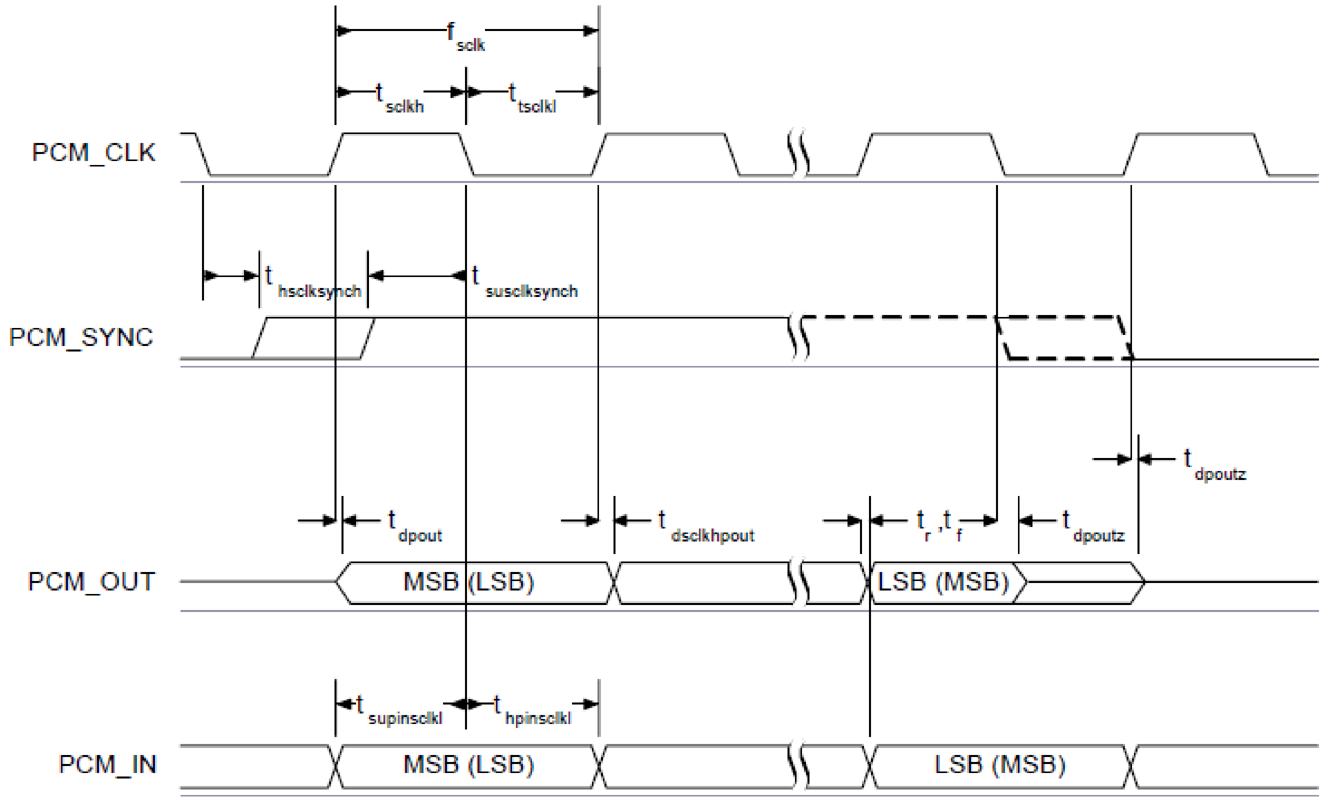
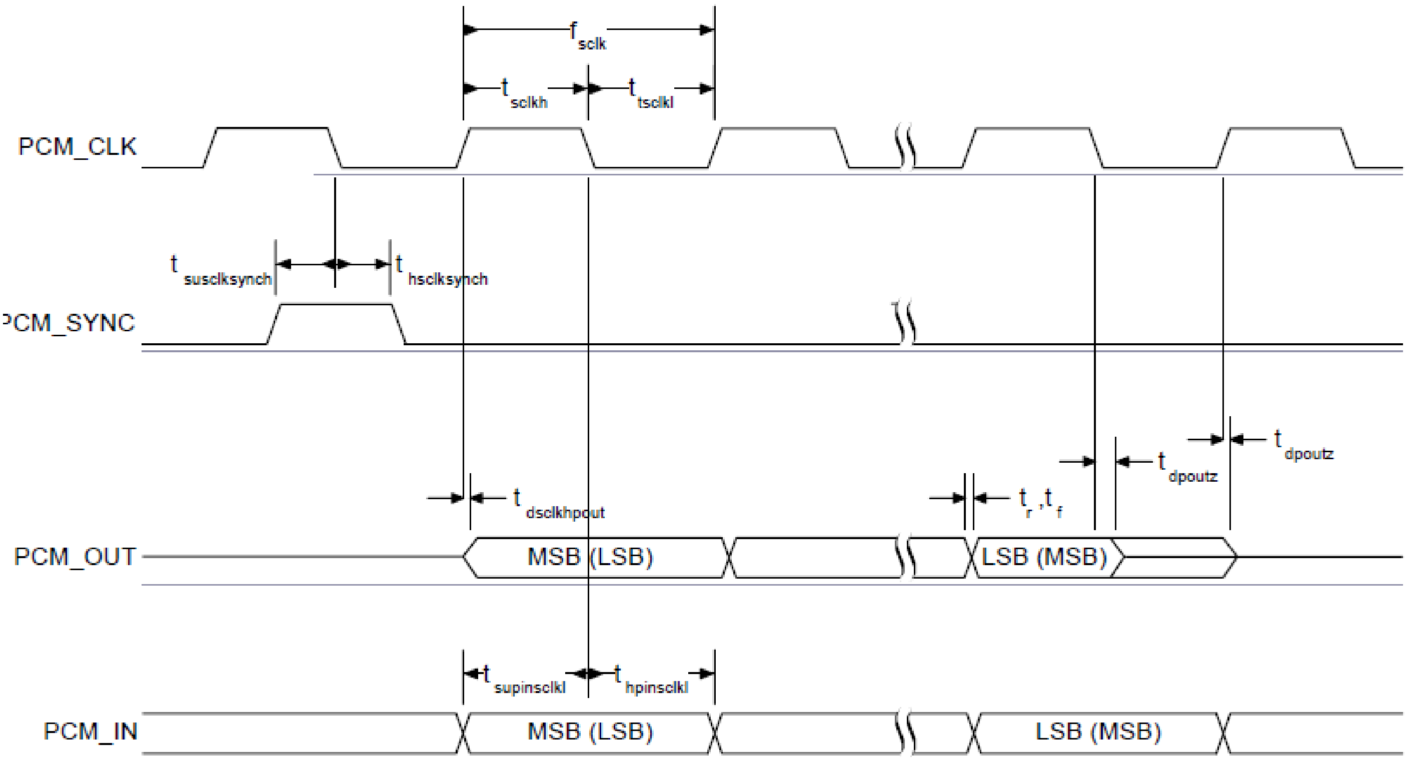


PCM Slave Timing Long Frame Sync



PCM Slave Timing Short Frame Sync

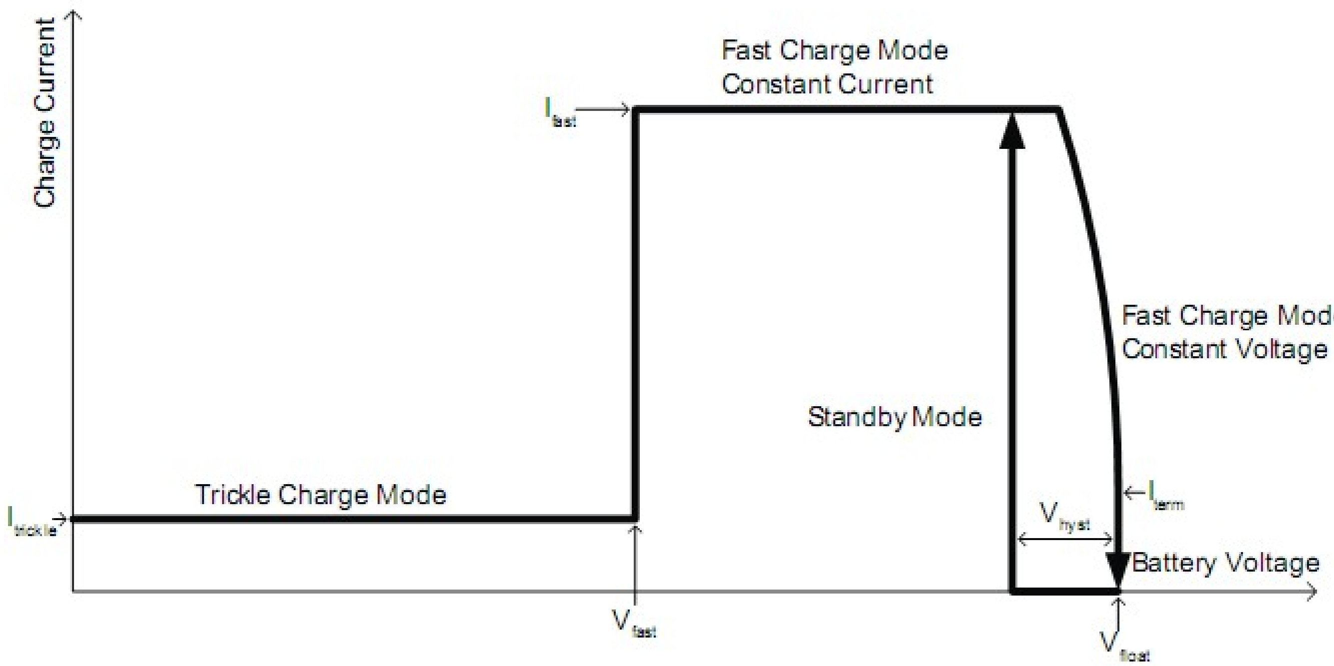
17. Battery Charger

The default mode for the SBC2015 battery charger is OFF. The battery charger hardware is enabled by the VM, The battery charger remains in a safe state. When enabled, the battery charger has 4 further operating modes:

- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current,

Mode	Battery Charger Enabled	VBAT_SENSE
Off	No	X
Trickle charge	Yes	>0 and <V_{fast}
Fast charge	Yes	>V_{fast} and <V_{float}
Standby	Yes	I_{term} [a] and >(V_{float} - V_{hyst})
Error	Yes	>(VCHG - 50mV)



Off Mode

In the off mode the battery charger is fully disabled and draws no active current on any of its terminals.

Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the Vfast threshold, a current of approximately 10% of the fast charge current, Ifast, is sourced from the VBAT pin. The Vfast threshold detection has hysteresis to prevent the charger from oscillating between modes. Current drawn from the VCHG input is the sum of the current sourced into the battery, IVCHG, plus an overhead of no more than 3.5mA.

Fast Charge Mode

When the voltage on VBAT_SENSE is greater than Vfast, the current sourced from the VBAT pin increases to Ifast. Ifast is between 10mA and 200mA set by PS Key or a VM trap. In addition, Ifast is calibrated in production test to correct for process variation in the charger circuit. The current is held constant at Ifast until the voltage at VBAT_SENSE reaches Vfloat, then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin. When the current sourced is below the termination current, Iterm, the charging stops and the charger enters standby mode. Iterm is typically 10% of the fast charge current.

Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at Vhyst below the final charging voltage, Vfloat, the charger re-enters fast charge mode.

Error Mode

The error mode is not entered during normal operation of the SBC2015. The charger enters the error mode when the voltage on the VCHG pin is too low to operate the charger correctly. The charger enters the error mode when the voltage on VBAT_SENSE is greater than VCHG - 50mV (typical). The battery charger does not require a reset to take it out of the error mode.

Battery Charger Trimming and Calibration

The battery charger default trim values are written by CSR into internal flash when each IC is characterised. CSR provides various PS Keys for overriding the default trims, VM Battery Charger Control The VM charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery

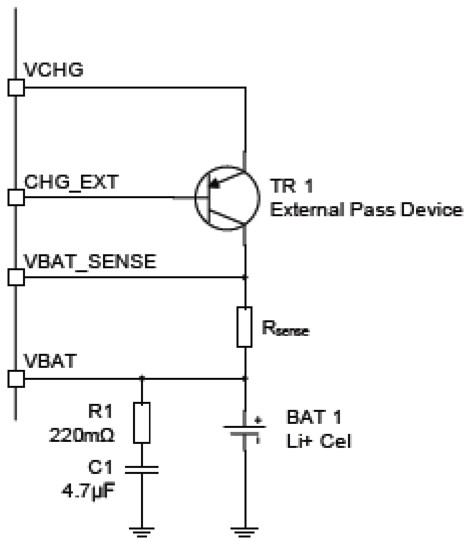
■ Monitoring the temperature of the die to protect against silicon damage
■ Monitoring the time spent in the various charge states
■ Enabling/disabling the charger circuitry based on the monitored information
■ Driving the user visible charger status LED(s)

Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and call traps from the VM charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys. For more information on the SBC2015, including details on setting up, calibrating, trimming and the PS Keys, see Lithium Polymer Battery Charger Calibration and Operation for SBC2015 application note.

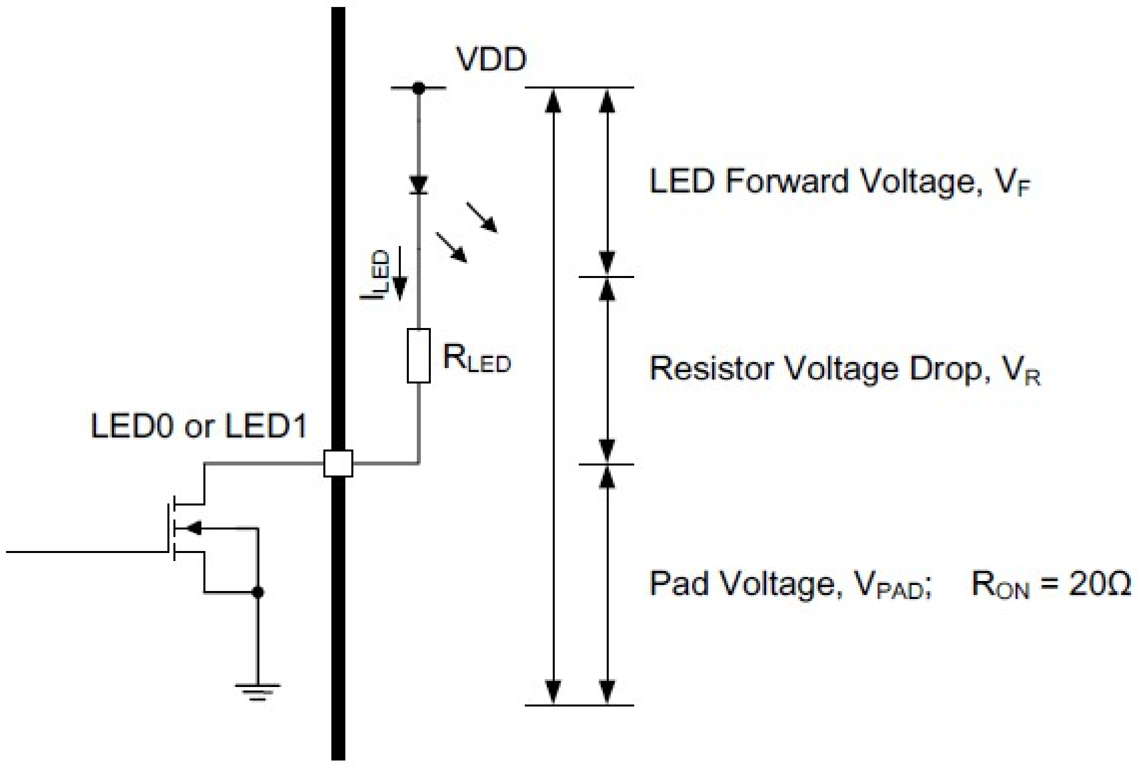
External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, Rsense, conneted in series with the external pass device, see Figure 12.2. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across Rsense is typically 200mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.



18. LED Drivers

SBC2015 includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware. The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.



LED Equivalent Circuit

it is possible to derive Equation 11.1 to calculate ILED or if a known value of current is required through the LED, to give a specific luminous intensity, then the value of RLED could be calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation11.1:LED Current

For LED[0] or LED[1] pad to act as resistance, the external series resistor, RLED, needs to be such that the voltagedrop across it, VR, keeps VPAD below 0.5V. Therefore Equation 11.2 also applies.

VDD = VF + VR + VPAD

Equation 11.2: LED PAD Voltage

Note:

The LED current will add to the overall application current, so conservative selection of the LEDs will preserve power consumption.

19. Reset (RST#)

SBC2015 is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. CSR recommends applying RST# for a period >5ms.

The power-on reset occurs when:

- The VDD_DIG supply falls below typically 0.97V or
- The VDD_AUX_1V8 supply falls below typically 1.46V

And is released when:

- VDD_DIG rises above typically 1.10V or
- VDD_AUX_1V8 rises above typically 1.65V

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.
Following a reset,
SBC2015 assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until SBC2015 is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in SBC2015 free runs, again at a safe frequency.

Digital Pin States on Reset

Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	Full Chip Reset
USB_DP	Digital bidirectional	N/A
USB_DN	Digital bidirectional	N/A
UART_RX	Digital bidirectional with PU	Strong PU

Pin Name / Group	I/O Type	Full Chip Reset
UART_TX	Digital bidirectional with PU	Weak PU
UART_CTS	Digital bidirectional with PD	Weak PD
UART_RTS	Digital bidirectional with PU	Weak PU
SPI_CS#	Digital input with PU	Strong PU
SPI_CLK	Digital input with PD	Weak PD
SPI_MISO	Digital tristate output with PD	Weak PD
SPI_MOSI	Digital input with PD	Weak PD
PCM_IN	Digital bidirectional with PD	Weak PD
PCM_OUT	Digital bidirectional with PD	Weak PD
PCM_SYNC	Digital bidirectional with PD	Weak PD
PCM_CLK	Digital bidirectional with PD	Weak PD
RST#	Digital input with PU	Strong PU
PIO[15:0]	Digital bidirectional with PD	Weak PD
QSPI_FLASH_IO[3:0]	Digital bidirectional with PD	Strong PD
QSPI_SRAM_CS#	Digital bidirectional with PU	Strong PU
QSPI_FLASH_CS#	Digital bidirectional with PU	Strong PU
QSPI_SRAM_CLK	Digital bidirectional with PD	Strong PD
QSPI_FLASH_CLK	Digital bidirectional with PD	Strong PD

Pin States on Reset

Status after Reset

The chip status after a reset is as follows:

■ Warm reset: data rate and RAM data remain available.

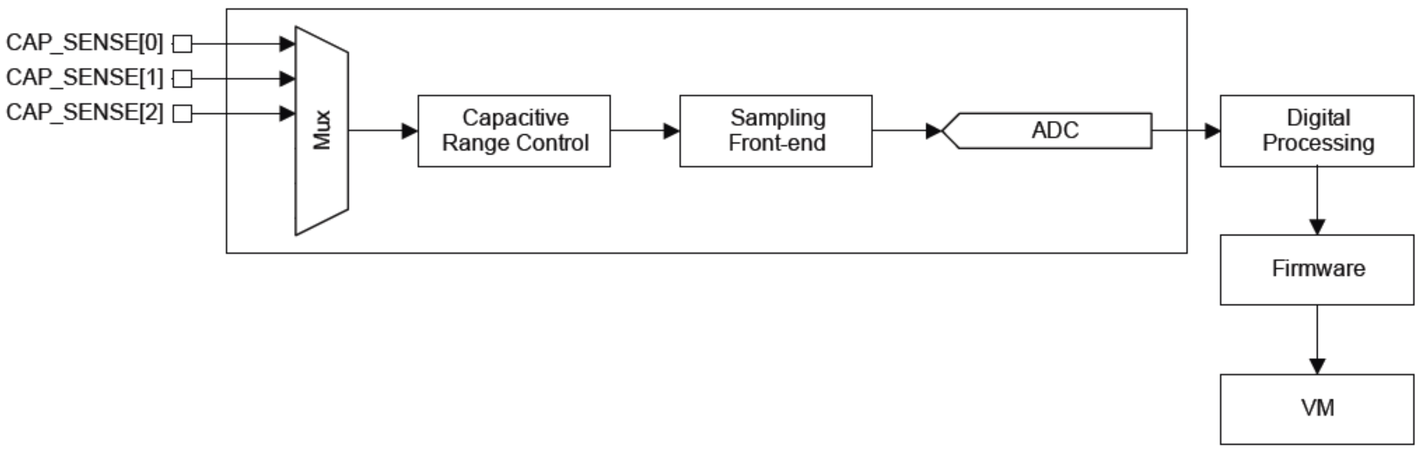
■ Cold reset: data rate and RAM data not available.

20. Capacitive Touch Sensor

capacitive touch sensor interface features:

■ Support for up to 3 capacitive touch sensing electrodes:
■ Printed on the PCB
■ Made from flex PCB
■ Configuration for individual buttons
■ Configuration for a wipe-type arrangement where 2 or more pads sense taps at each end or a wipe from one side to the other
■ Operates in deep sleep and is a programmable source for wake-up

Figure shows the system block diagram for the capacitive touch sensor interface. The interface depends on the capacitive touch sensor type. Therefore the overall control of the capacitive touch sensor interface resides in the VM, so it is easily modified in each end-user application.



21. Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v3.0 + EDR specification functionality:

■ Secure simple pairing
■ Sniff subrating
■ Encryption pause resume
■ Packet boundary flags
■ Encryption
■ Extended inquiry response

As well as the following mandatory functions of Bluetooth v2.0 + EDR specification:

■ AFH), including classifier

■ Faster connection: enhanced inquiry scan (immediate FHS response)
■ LMP improvements
■ Parameter ranges
■ Has on-chip software that can be loaded with applications from CSR's eXtension Program

And optional Bluetooth v3.0 + EDR specification functionality:
■ AFH as Master and Automatic Channel Classification
■ Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
■ eSCO), eV3 +CRC, eV4, eV5
■ SCO handle
■ Synchronisation
The firmware was written against the Bluetooth v3.0 + EDR specification:
■ Bluetooth components:
■ Baseband (including LC)
■ LM
■ HCI
■ Standard UART HCI Transport Layers
■ All standard Bluetooth radio packet types
■ Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps
■ Operation with up to seven active slaves2
■ Scatternet v2.5 operation
■ Maximum number of simultaneous active ACL connections: 7
■ Maximum number of simultaneous active SCO connections: 33
■ Operation with up to three SCO links, routed to one or more slaves
■ All standard SCO voice coding, plus transparent SCO
■ Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
■ All standard pairing, authentication, link key and encryption operations
■ Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
■ Dynamic control of peers' transmit power via LMP
■ Master/Slave switch
■ Broadcast
■ Channel quality driven data rate
■ All standard Bluetooth test modes

Bluetooth Profiles:
■ Bluetooth v3.0 specification support
■ HFP v1.6
■ HSP v1.2
■ A2DP v1.2

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- AVRCP v1.4
- PBAP v1.0
- MAP v1.0
- SPP v1.0 (on demand)
- Improved Audio Quality:
- CVC 1-mic far-end audio enhancements (narrowband)
- CVC 2-mic far-end audio enhancements (narrowband)
- CVC 1-mic far-end audio enhancements (hands-free)
- CVC 1-mic far-end audio enhancements (wideband)
- CVC 2-mic far-end audio enhancements (wideband)
- CVC near-end audio enhancements
- PLC / BEC
- 1-mic WNR
- 2-mic WNR
- Sidetone
- Frequency expansion for improved speech intelligibility
- Music Enhancements:
- aptX codec technology
- 5-band EQ
- 3D stereo separation
- Dynamic range control
- Faststream codec
- SBC decoder
- MP3 decoders
- AAC and AAC+ decoders
- Stereo Ambient Noise Cancellation
- Additional Functionality:
- Multipoint for HFP, A2DP and advance user-cases
- Programmable audio prompts (compressed / SBC)
- Support for capacitive touch control
- Support for speech recognition
- Support for multi-language programmable audio prompts
- CSR's proximity pairing and CSR's proximity connection
- Multipoint support for HFP connection to 2 handsets for voice
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- Talk-time extension

22. Software specification

Software function

(a) SBC2015-SD

SBC2015-SD is the Smart Drive sfotware. This software will perform SBC2015 module itselves. There is no software effort by user to control this module after ponwe on.

support Profile

Stack / Profile	SBC2015-SD BT3.0 module
A2DP	V
HSP	V
HFP	V
AVRCP	V

(b) SBC2015-AT

SBC2015-AT will act only when you send AT command. Detailed AT command, please check the document “A2DP_AT_Commands”

support Profile

Stack / Profile	SBC2015-AT BT3.0 module
A2DP	V
HSP	V
HFP	V
AVRCP	V
MAP	(under Request)
PBAP	(under Request)
SPP	(under Request)

23. Default setting Information

		Parameter
1	Baud Rate	
2	Pin Code Prompt	
3	Local Name	
4	Master/Slave	

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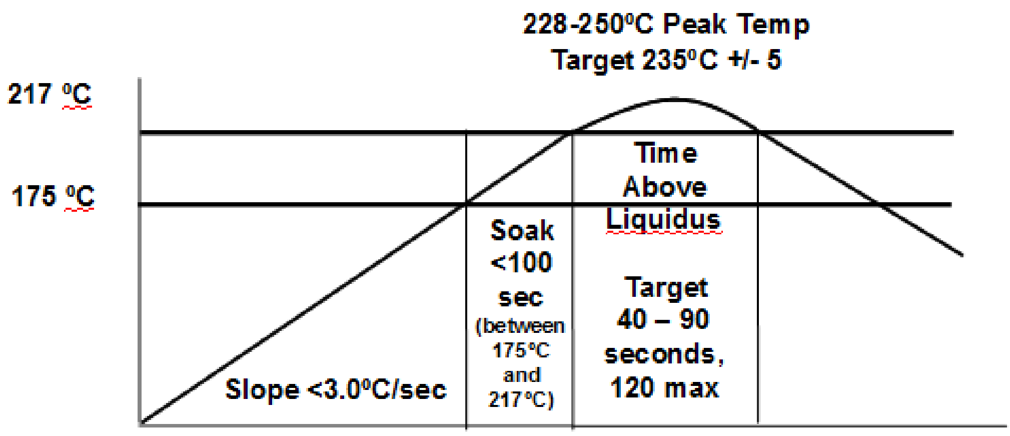
24. Reflow information

Reflow Profile Graphic, assuming:

1. Kester R905 Sn/4Ag/0.5Cu solder paste.
2. All solder ball alloys melt at 217°C.
3. Component joints do not exceed temperatures as per J-STD-02



Federal Communications Commission (FCC) Statement

15.21

You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

15.105(b)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
1) this device may not cause interference and
2) this device must accept any interference, including interference that may cause undesired operation of the device.